

Claims

What is claimed is:

- 5 1. An apparatus for interconnecting a semiconductor die to a printed circuit board, comprising:
a substrate;
a conductive trace formed on the substrate having a first surface area,
the first surface area being of a first solderability;
10 a conductive pad formed on the first surface area of the conductive trace having a second surface area, the second surface area being of a second solderability, the second solderability is greater than the first solderability; and
wherein a solder bump on the semiconductor die can be connected to
15 the second surface area without using another material to contain the solder on the second surface area.
2. The apparatus of claim 1, wherein a dielectric portion of the substrate is formed of an organic material.
- 20 3. The apparatus of claim 1, wherein the conductive trace comprises copper.
4. The apparatus of claim 1, wherein the conductive pad has a layer that comprises gold.
- 25 5. The apparatus of claim 4, wherein the conductive pad has a layer that comprises nickel between the layer comprising gold and the conductive trace.
- 30 6. The apparatus of claim 1, wherein the solder bump on the semiconductor die is connected to the second surface area without using a soldermask to contain the solder on the second surface area.

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7. The apparatus of claim 1, wherein a native oxide of the first surface area adjacent to the second surface area increases a differential solderability between the first and second surface areas to inhibit the solder from flowing over the first surface area.

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8. The apparatus of claim 1, wherein the conductive trace is oxidized to reduce a relative solderability of the conductive trace as compared to conductive pad.

- 10 9. The apparatus of claim 1, wherein the second surface area is for connecting to a eutectic tin-lead solder bump.

10. A method for electrically connecting a semiconductor die to a substrate, comprising the steps of:

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forming a conductive trace on the substrate, the conductive trace comprising a first metal;

defining a surface area of the conductive trace on which to form a conductive pad; and

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forming the conductive pad comprising a second metal, the second metal having greater solderability than the first metal;

wherein a solder bump for electrically connecting the semiconductor die to the substrate, when melted, will not flow onto the first metal.

- 25 11. The method of claim 10 wherein the conductive trace is formed of copper.

12. The method of claim 10 wherein the conductive pad is formed using gold plating.

- 30 13. The method of claim 10 wherein the step of forming the conductive trace includes forming the conductive trace having a surface comprising a native oxide and the step of forming the conductive pad includes forming the conductive pad of gold.

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- 5 14. A substrate for supporting a semiconductor die, comprising:
a copper trace for transmitting an electrical signal to or from the semiconductor die;
a gold pad formed on the copper trace, the gold pad for being a solderable connection to the semiconductor; and
wherein a surface of the copper trace has a relatively lower solderability than a surface of the gold pad, thereby allowing a solder bump to be melted and reflowed without the use of a soldermask to contain the solder while the solder is in a liquid state.
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15. The substrate of claim 14, wherein a dielectric portion of the substrate is formed from an organic material.
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16. The substrate of claim 14, wherein the gold pad has a layer that comprises nickel positioned between the gold pad and the copper trace.
17. The substrate of claim 14, wherein the copper trace includes a native oxide surface layer that increases a differential solderability between the gold pad and the copper trace.
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18. The substrate of claim 14, wherein the copper trace is oxidized to have an oxide layer formed on the surface of the copper trace to further reduce solderability of the copper trace.
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